UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,388	10/24/2003	Luiz Andre Barroso	200301825-5	2524

7590 01/27/2005

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
LI, ZHUO H	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,388	BARROSO ET AL.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-16,18-23 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-16,18-23 and 26-33* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed on 11/12/2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-4, 7, 9-10, 13, 15-16, 18-23 and 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ignatowski et al. (US PAT. 6,457,100 hereinafter Ignatowski) in view of Lentz et al. (US PAT. 5,440,752 hereinafter Lentz).

Regarding claim 1, Ignatowski discloses a chip-multiprocessing system with scalable architecture (41, figure 3), comprising on a single chip, a plurality of processor cores (15-1 – 15-N, figure 3), a two level cache hierarchy including a first level caches as private cache for each related processor (col. 8 lines 24-35), a second level cache with a relaxed inclusion property (40, figure 3), the second-level cache, i.e., common cache (40, figure 3) being logically shared by the plurality of processor cores (col. 9 lines 8-10), the second level cache being modular with a plurality of interleaved modules (col. 16 lines 33-40 and col. 18 lines 40-46), one or more memory controllers (4, figure 1) capable of operatively communicating with the two-level cache hierarchy and with an off-chip memory (col. 4 line 58 through col. 7 line 24), a cache coherence protocol, one or more coherence protocol engines, i.e., nodal directory, (col. 9 line 64 through col. 10 line 24), an intra-chip switch, i.e., an electronic cross point-type switch, and interconnect subsystem, i.e., inter-node bus. Although Ignatowski differs from the claimed invention in not specifically teaches the first level caches comprising a pair of instruction and data caches. It is well known in the art that the first level cache comprising both data and instruction caches for faster execute and access by the central processor, as an example of Lentz teaches in the multiple processing system (1, figure 1), each processors comprising a data cache 51 and an instruction cache 52 (figure 2 and col. 6 line 65 through col. 7 line 19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multiple processing system of Ignatowski in having a pair of data and instruction cache as the first level cache, as per teach of Lentz because it reduces the latency of memory accesses and speed up an access by any processor with their private data and instruction caches.

Regarding claim 2, Ignatowski discloses a chip-multiprocessing system wherein the scalable architecture is targeted at parallel commercial workloads (col. 4 line 58 through col. 7 line 8).

Regarding claim 3, Ignatowski discloses a chip-multiprocessing system further comprising on a single I/O chip, a processor core similar in structure and function to the plurality of processor cores (col. 8 lines 23-35), a single-module second level cache (40, figure 3) with controller (27, figure 3), an I/O router (col. 12 line 52 col. 3 line 7), and a memory that participates in the cache coherency protocol (28-1 – 28-M, figure 3 and col. 15 line 48 through col. 16 line 9).

Regarding claim 4, Ignatowski discloses a chip-multiprocessing system wherein the plurality of core processors are each a single-issue, in-order processor configured with a pipelined data path and hardware support for floating-point operations (col. 4 line 58 through col. 7 line 8).

Regarding claim 7, Lentz discloses a chip-multiprocessing system wherein each of the plurality of processor cores is capable of separately interfacing (55 and 56, figure 2) with either of the instruction and data caches, and wherein each of the caches is configured for single-cycle latency (col. 7 line 29 through col. 8 line 14).

Regarding claim 9, Ignatowski discloses a chip-multiprocessing system wherein the single chip creates a node, and wherein the coherence protocol engines include a home engine and a remote engine which support shared memory across multiple nodes (col. 9 line 26 through col. 10 line 35).

Regarding claim 10, Ignatowski discloses a chip-multiprocessing system further comprising a system control module that takes care of system initialization and maintenance including configuration, interrupt handling, and performance monitoring (col. 4 line 58 through col. 7 line 8).

Regarding claim 13, the difference between Lentz and the claims is the claims specifically recite the second level cache is interleaved into eight modules. However, having this sized memory does not have a disclosed purpose nor is this size disclosed to overcome any deficiencies in the prior art. As such, the memory may have been of any size. In addition, since Lentz teaches the cache is able to program and interleave (col. 7 lines 3-28), the ordinary artisan would realize a possible memory size increase, as the current technology would warrant. Accordingly, it would have been an obvious matter of design choice to utilize the system of Lentz wherein the cache is interleaved into vary size, as disclosed supra, since applicant has not disclosed that an interleaved eight modules, as opposed to other sizes, overcomes a deficiency in the prior art or is for any stated purpose.

Regarding claim 15, Lentz discloses a chip-multiprocessing system wherein each instruction cache is kept coherent by hardware (col. 7 lines 3-19).

Regarding claim 16, Ignatowski discloses a chip-multiprocessing system wherein each of the second level cache modules includes an N-way set associative cache and use a round-robin or least-recently-loaded replacement policy if an invalid block is not available (col. 9 lines 8-24).

Regarding claim 18, Ignatowski discloses a chip-multiprocessing system wherein the pair of instruction and data caches includes a first state field per each cache line present therein the first state field having bits related to the MESI (col. 14 lines 33-41 and col. 16 lines 41-55).

Regarding claims 19-20, Ignatowski discloses a chip-multiprocessing system wherein the second level cache maintains a duplicate of the first state fields from the first-level cache pairs of instructions and data caches, the duplicate being maintained in order to avoid the need for a first-level cache lookup for cache lines that map to given addresses of corresponding requested cache lines and the second level cache holds a second state field for each cache line present therein, the second state field having bits related to the MESI protocol, wherein the second level cache maintains a duplicate of the first state field, and wherein on every second level cache access the duplicate first state fields and the second state fields are accessed in parallel (col. 16 line 41 through col. 17 line 12 and col. 17 line 56 through col. 18 line 28).

Regarding claim 21, Ignatowski discloses a chip-multiprocessing system wherein the single chip creates a node (41-1 – 41-4, figure 4), and wherein information about sharing of data across nodes in kept in a directory in a memory accessed via the memory controllers (col. 18 line 47 through col. 19 line 26).

Regarding claim 22, Ignatowski discloses a chip-multiprocessing system wherein the second level cache includes a controller (27, figure 3), and wherein manipulation and interpretation of the directory is done by the protocol engines, although the controller also interprets the directory, but merely for determining whether a cache line is cached remotely to the single chip (col. 15 line 48 through col. 16 line 40).

Regarding claim 23, Ignatowski discloses a chip-multiprocessing system wherein the interconnect subsystem includes at least one data path (33A and 33B, figure 5), and wherein the interconnect subsystem is a crossbar configured with a uni-directional, push-only interface, and is capable of scheduling data transfers according to data paths availability, pre-allocating data

paths, speculatively asserting a requester's grant single, and supporting back-to-back transfer without dead-cycles between transfers (col. 21 line 60 through col. 22 line 8).

Regarding claim 26, Ignatowski discloses a chip-multiprocessing system wherein the memory controller includes a memory access controller with high-speed interface circuitry and a memory controller engine capable of scheduling second-level cache memory access (col. 15 line 48 through col. 16 line 32).

Regarding claim 27, Ignatowski discloses a chip-multiprocessing system wherein the coherence protocol engines are implemented as similarly structured micro-programmable controllers, although each of them as its respective micro-code (col. 16 line 41 through col. 17 line 19).

Regarding claim 28, Ignatowski discloses a chip-multiprocessing system wherein each of the coherence protocol engines is corresponding to determine the requested data and/or instruction in the coherence protocol (MESI). Although Ignatowski failed to clearly discloses the coherence protocol engines is configured with an input state, a microcode-controlled execution stage and an output stage. It recognizes that a step of a requested data from processor to compare the status in the coherence protocol engines as an input stage, a step of determine the status of requested data by MESI protocol as a microcode-controlled execution stage, and a step of output the status of the requested data as an output stage (col. 17 line 56 through col. 19 line 1).

Regarding claim 29, the difference between Ignatowski and the claims is the claims specifically recite the protocol code that includes instructions named Send, Receive, Lsend, Lreceive, Test, Set and Move. However, having the special instruction name does not have a

disclosed purpose nor is this names disclosed to overcome any deficiencies in the prior art. As such, the instruction name may have been of vary name. In addition, since Ignatowski discloses the directory information (hit, miss, exclusive, modified, invalid, etc...) at col. 17 lines 13-19. Accordingly, it would have been an obvious matter of design choice to utilize the system of Ignatowski wherein the protocol code (hit, miss, exclusive, modified, invalid, etc...), as disclosed supra, since applicant has not disclosed that the instructions named Send, Receive, Lsend, Lreceive, Test, Set and Move, as opposed to other names, overcomes a deficiency in the prior art or it for any stated purpose.

Regarding claim 30, Regarding claim 1, Ignatowski discloses a chip-multiprocessing system with scalable architecture (41, figure 3), comprising on a single chip, a plurality of processor cores (15-1 – 15-N, figure 3), a two level cache hierarchy including a first level caches as private cache for each related processor (col. 8 lines 24-35), a second level cache with a relaxed inclusion property (40, figure 3), the second-level cache, i.e., common cache (40, figure 3) being logically shared by the plurality of processor cores (col. 9 lines 8-10), the second level cache being modular with a plurality of interleaved modules (col. 16 lines 33-40 and col. 18 lines 40-46), one or more memory controllers (4, figure 1) capable of operatively communicating with the two-level cache hierarchy and with an off-chip memory (col. 4 line 58 through col. 7 line 24), a cache coherence protocol, one or more coherence protocol engines, i.e., nodal directory, (col. 9 line 64 through col. 10 line 24), an intra-chip switch, i.e., an electronic cross point-type switch, and interconnect subsystem, i.e., inter-node bus, the single chip creates a node (41-1 – 41-4, figure 5) and providing one ore more than one of the nodes to create in a modular scalable fashion, a glueless multiprocessor (col. 22 line 18-63) . Although Ignatowski differs from the

claimed invention in not specifically teaches the first level caches comprising a pair of instruction and data caches. It is well known in the art that the first level cache comprising both data and instruction caches for faster execute and access by the central processor, as an example of Lentz teaches in the multiple processing system (1, figure 1), each processors comprising a data cache 51 and an instruction cache 52 (figure 2 and col. 6 line 65 through col. 7 line 19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multiple processing system of Ignatowski in having a pair of data and instruction cache as the first level cache, as per teach of Lentz because it reduces the latency of memory accesses and speed up an access by any processor with their private data and instruction caches.

Regarding claim 31, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 32, the limitation of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 33, although Ignatowski does not clearly disclosures each of the plurality of interleaved modules of the second level cache comprises dedicated tag and data storage, Ignatowski teaches the interleaves nodal directory (24, figure 2) is under set-associative structure (col. 16 lines 33-40), and it is well known in the art that the set-associative memory comprises tag and data storage. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize the interleaves nodal directory comprises dedicated tag and data storage.

4. Claims 5-6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ignatowski et al. (US PAT. 6,457,100 hereinafter Ignatowski) and Lentz et al. (US PAT. 5,440,752 hereinafter Lentz) as applied to claim 1 above, and further in view of Dean et al. (US PAT. 6,202,127 hereinafter Dean).

Regarding claims 5-6, the combination of Ignatowski and Lentz differs from the claimed invention in not specifically teaches the chip-multiprocessing system wherein the plurality of processor cores are each capable of executing an instructions set of the ALPHA™ processing core and each configured with a branch target buffer, pre-compute logic for ranch conditions, and a fully bypassed data path. However Dean teaches such (col. 2 lines 61-65 and col. 3 line 56 through col. 3 line 7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Ignatowski and Lentz in having the plurality of processor cores are each capable of executing an instructions set of the ALPHA™ processing core and each configured with a branch target buffer, pre-compute logic for ranch conditions, and a fully bypassed data path, as per teaching of Dean, because it implements the chip-multiprocessing system and reduces memory latency.

Regarding claim 14, the combination of Ignatowski and Lentz differs from the claimed invention in not specifically teaches the chip-multiprocessing system wherein each of the instruction and data caches is a two-way set-associative cache with virtual indices and physical tags. However Dean teaches such (col. 3 line 20 through col. 4 line 21). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Ignatowski and Lentz in having each of the instruction and data

caches is a two-way set-associative cache with virtual indices and physical tags, as per teaching of Dean, because it implements the chip-multiprocessing system and reduces memory latency.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ignatowski et al. (US PAT. 6,457,100 hereinafter Ignatowski) and Lentz et al. (US PAT. 5,440,752 hereinafter Lentz) as applied to claim 1 above, and further in view of Eng et al. (US PAT. 5,467,679 hereinafter Eng).

Regarding claim 8, the combination of Ignatowski and Lentz differs from the claimed invention in not specifically teaches the chip-multiprocessing system wherein the interconnect subsystem includes a network router, a packet switch and input and output queues. However, Eng teaches such (col. 4 line 41 through col. 5 line 31). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Ignatowski and Lentz in having the interconnect subsystem includes a network router, a packet switch and input and output queues, as per teaching of Eng, because it reduces buffer space and increase throughput is achieved by providing shared memory.

Allowable Subject Matter

6. Claim 12 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 1-10,12-16,18-23 and 26-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on M-F 9:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
Art Unit 2186

MATTHEW ANDERSON
PRIMARY EXAMINER
GROUP 2100